UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,277	07/25/2003	Tae W. Kim	OF03P106/US	4246

36872 7590 02/13/2004

THE LAW OFFICES OF ANDREW D. FORTNEY, PH.D., P.C.
7257 N. MAPLE AVENUE
BLDG. D, 3107
FRESNO, CA 93720

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,277	KIM, TAE W.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/627,277. Currently, claims 1-8 are pending.

Drawings

2. Figures 1A-1C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it is not limited to a single paragraph within the range of 50 to 150 words. Furthermore, the abstract contains the following legal phraseology often used in patent claims: "comprising" (page 13, line 6). Correction is required. See MPEP § 608.01(b).

4. The specification is objected to because of the following informalities: it is unclear what unit of measurement the symbol □ represents, (e.g. angstroms (Å), nanometers (nm), microns (μm)) (page 6, line 22); and the term "field stop" should be "punch stop" (page 7, line 8). Appropriate correction is required.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 2-8 are objected to because of the following informalities: the word "of" should be changed to "on" (claim 2, line 9). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification does not provide support for conducting ion implantations for field stop formation only under the to-be-gate electrode area, as recited in claim 3. Instead, the specification provides support for conducting ion implantations for threshold voltage adjustment and punch stop formation only under the to-be-gate electrode area. See specification - page 7, lines 4-7.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 2-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear what is meant by the phrase "forming a gate oxide layer on the surface of the substrate *under* the bottom face of the trench" as recited in claim 2, line 17.

It is unclear what unit of measurement the symbol □ represents, e.g. angstroms (Å), nanometers (nm), microns (μm) (claim 5).

Claims 3-6 depend from claims 1 and 2 in the alternative. However, claim 1 does not provide antecedent basis for the limitations recited in claims 3-8 (e.g. "the to-be-gate

electrode area" (claim 3, line 3), and "the sacrificial layer" (claim 4, line 2). It is suggested that claims 3-6 be amended to depend from claim 2 only.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. *Claims 1, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Stolmeijer et al. (US 5,384,279).*

The Stolmeijer et al. patent (Stolmeijer) discloses a method for fabricating MOS transistors (figs. 1-5 and accompanying text). The method comprises the following steps substantially as claimed: forming a buffer oxide layer 16 on a semiconductor substrate 2 (fig. 1 and col. 8, lines 49-54) having an isolation layer 7 (fig. 1 and col. 5, lines 38-44); and conducting ion implantations for n-well formation, p-well formation, and field stop formation in an active region of the substrate through the buffer oxide layer 16 (figs. 1 and 2). For n-well formation, see fig. 1 and col. 6, lines 53-61. For p-well formation, see fig. 2 and col. 6, line 66 - col. 7, line 7. For field stop formation see figs. 1, 2, and col. 9, lines 25-34. For ion implantation for well formation and field stop formation in an active region of the substrate through the buffer oxide layer 16, see col. 8, lines 49-52.

The ion for well formation and field stop formation is boron, phosphorous or arsenic, as recited in claim 7 (col. 6, lines 54-61; col. 7, lines 1-7; and col. 9, lines 25-34).

The implant for field stop formation is made at a sufficient energy to form barriers below the source/drain junctions 22, 24 (fig. 5).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. *Claims 2, 3, 5, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shao et al. (US 6,410,394 B1) in view of Stolmeijer et al. (US 5,384,279).*

Claim 2 insofar as in compliance with 35 USC 112, second paragraph is unpatentable over Shao et al. in view of Stolmeijer et al. The Shao et al. patent (Shao) discloses a method for fabricating MOS transistors (see figs. 1A,1B, 2A, 2B, 3, and 4 and accompanying text). The method comprises the following steps recited in claim 2: providing a semiconductor substrate 11 (fig. 1A); forming isolation layers 12, wherein the isolation layers is either shallow trench isolation (STI) or field oxide formed by local oxidation of silicon (LOCOS) (fig. 1A and col. 3, lines 19-22); forming a p-well and an n-well in active regions 13 and 15 of the substrate, respectively (col. 3, lines 23-33); forming a sacrificial layer 30 on the semiconductor substrate (fig. 1A and col. 3, lines

39-43); patterning the sacrificial layer to form trenches defining gate electrode forming regions (fig. 1B); conducting ion implantations for threshold voltage adjustment and punch stop formation on the semiconductor substrate area exposed by the trenches (fig. 2A and col. 4, lines 4-56); forming a gate oxide layer 20 on the surface the substrate under the bottom face of the trenches (fig. 1B); forming a conductive layer on the sacrificial layer so as to completely bury the trench, wherein the conductive layer can be a doped polysilicon layer (col. 4, lines 57-61); polishing the conductive layer until the surface of the sacrificial layer is exposed, so as to form gate electrodes 40 and 50 (fig. 3 and col. 4, lines 64-67); removing the sacrificial layer 30 (col. 5, lines 1-4); forming LDD regions 43 and 42 in the surface of the substrate at both side portions of gate electrodes 40 and 50, respectively (fig. 4); forming spacers 44 on both side walls of gate electrodes 40 and 50 (fig. 4); and forming the source/ drain regions 47 and 46 in the surface of the substrate at both side portions of gate electrodes 40 and 50, respectively, including the spacers 44 (fig. 4).

Claim 3 insofar as in compliance with 35 USC §112, first paragraph is rejected over Shao in view of Stolmeijer. The implantations for punch stop formation are conducted only under the to-be-gate electrode area.

Boron, phosphorus, and arsenic ions are used for well formation and field stop formation, as recited in claim 7 (col. 4, lines 4-56).

As discussed above, the Shao patent discloses the steps of providing a semiconductor substrate 11; forming isolation layers 12, which is either STI or field

oxide; and forming twin wells. However, Shao lacks anticipation in not teaching the following limitations, as recited in claim 2: forming a buffer oxide layer on the semiconductor substrate; forming the n-well and the p-well by conducting ion implantations through the buffer oxide layer; forming field stop regions, wherein the field stop regions are formed by conducting ion implantations through the buffer oxide, and wherein the implant for field stop formation is made at a sufficient energy to form barriers below the source/ drain junction, as recited in claim 8; and removing the buffer oxide layer.

Again, Stolmeijer discloses a method for fabricating MOS transistors. As previously explained, Stolmeijer discloses the following steps (see the rejection of claim 1 addressed in Section No. 5 of this action): forming a buffer oxide layer 16 on a semiconductor substrate 2 having an isolation layer 7 (fig. 1); and conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer (figs. 1 and 2). The method further comprises a step of removing the buffer oxide layer (fig. 3 and col. 8, lines 49-54). The implant for field stop formation is made at a sufficient energy to form barriers below the source/ drain junctions 22 and 26 (fig. 4 and col. 9, lines 31-34).

Since both the Shao patent and the Stolmeijer patent are from the same field of endeavor, the purpose disclosed by Stolmeijer would have been recognized in the pertinent reference of Shao by one having ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Shao in view of Stolmeijer for reasons as follows: when the isolation layer 12 (Shao) is field oxide, forming field stop regions, as taught by Stolmeijer, prevents the formation of parasitic transistors below the field oxide regions (Stolmeijer - col. 9, lines 31-34); forming a buffer oxide layer on the substrate, and conducting ion implantations through the buffer oxide layer for formation of the n-well, the p-well, and field stop regions, as taught by Stolmeijer, prevents contamination of the substrate during the implanting step; and removing the buffer oxide layer, as taught by Stolmeijer, provides a clean surface for the subsequent growth of a substantially thin gate oxide layer (Stolmeijer - col. 8, lines 52-54).

Claim 5 insofar as in compliance with 35 USC 112, second paragraph is unpatentable over Shao in view of Stolmeijer. While Shao teaches that the sacrificial layer 30 has a thickness ranging from between about 2000 to 4000 A (col. 3, lines 40-43), Shao does not teach that the sacrificial layer is formed to a thickness ranging from between 500 A and 1000 A. However, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the sacrificial layer to a thickness ranging from between 500 A and 1000 A, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art (In re Aller,105 USPQ 233).

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shao in view of Stolmeijer as applied to claim 2 above, and further in view of Squillace et al. (3,859,222).

While Shao teaches the patterning of sacrificial layer 30, which is preferably composed of silicon nitride, using a reactive ion etching (RIE) process (i.e. dry-etching process) (col. 3, lines 58-62), Shao does not teach that the patterning of the sacrificial layer is implemented via a wet-etching process, as recited in claim 6.

The Squillace et al. patent (Squillace) discloses a method for etching a silicon nitride layer and a silicon oxide layer (figs. 1a-1c and accompanying text). The method comprises a step of patterning a silicon nitride layer 14 using a wet-etching process (fig. 1c and col. 2, line 64 - col. 3, line 7).

Since the Shao patent and the Squillace patent are from the same field of endeavor, the purpose disclosed by Squillace would have been recognized in the pertinent reference of Shao by one having ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Shao and Stolmeijer in view of Squillace, by patterning the sacrificial layer of silicon nitride using a wet-etching process in place of an RIE process, since the wet-etching process creates a smooth slope on the sidewalls of the trench.

Allowable Subject Matter

12. *Claim 4 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of base claim 2 and any intervening claims.* Shao teaches away from using a sacrificial layer composed

of an oxide layer (col. 3, lines 56-67). The trenches are formed in the sacrificial layer 30 using an etchant that has a high selectivity of the sacrificial layer 30 to the gate insulating layer 20. Since the gate insulating layer 20 is composed of oxide, the sacrificial layer 30 cannot be an oxide layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1675.

TMT
21 January 2004

Michael Trinh
Primary Examiner
Art SPE
1/26/04